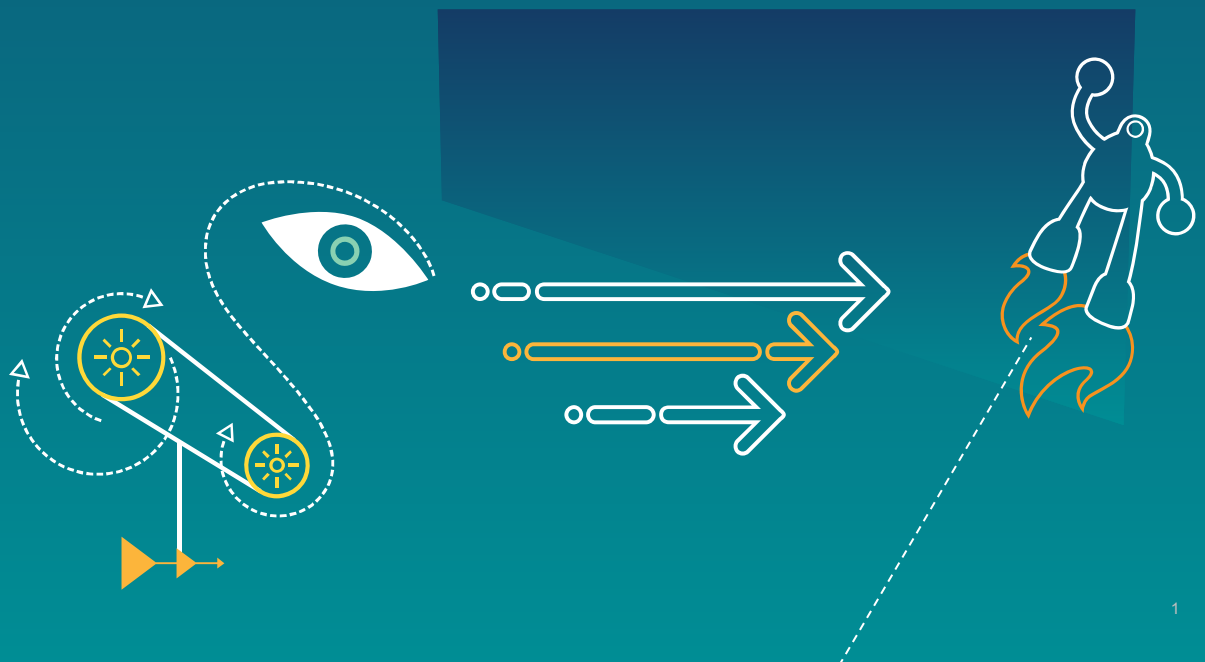
Speaker name
Job title, date, legal entity

layout feedback
April 19th



Stackup change

We switched to different PWB manufacturer.

Need to update all the control impedance traces in all the layers

Waivers - Customer approval of stackup includes approval of:

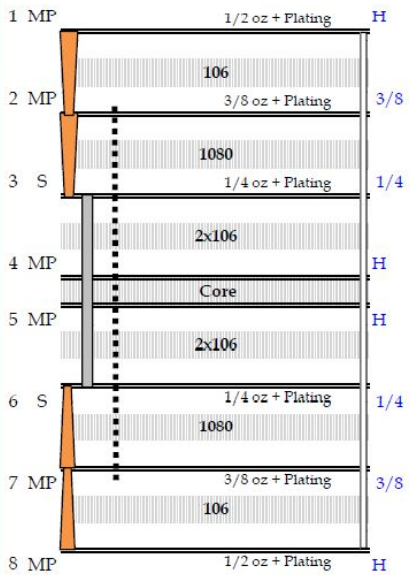
Notes / Comments:

1- Please include approved stackup with final data set.

Stacked micro vias: Layers 1-2, 2-3, 7-6 and 8-7 to be copper filled

Buried vias: Layers 3-6 will be non conductive epoxy filled.

Indicates a Dummy Sub. (TTM's internal use only)



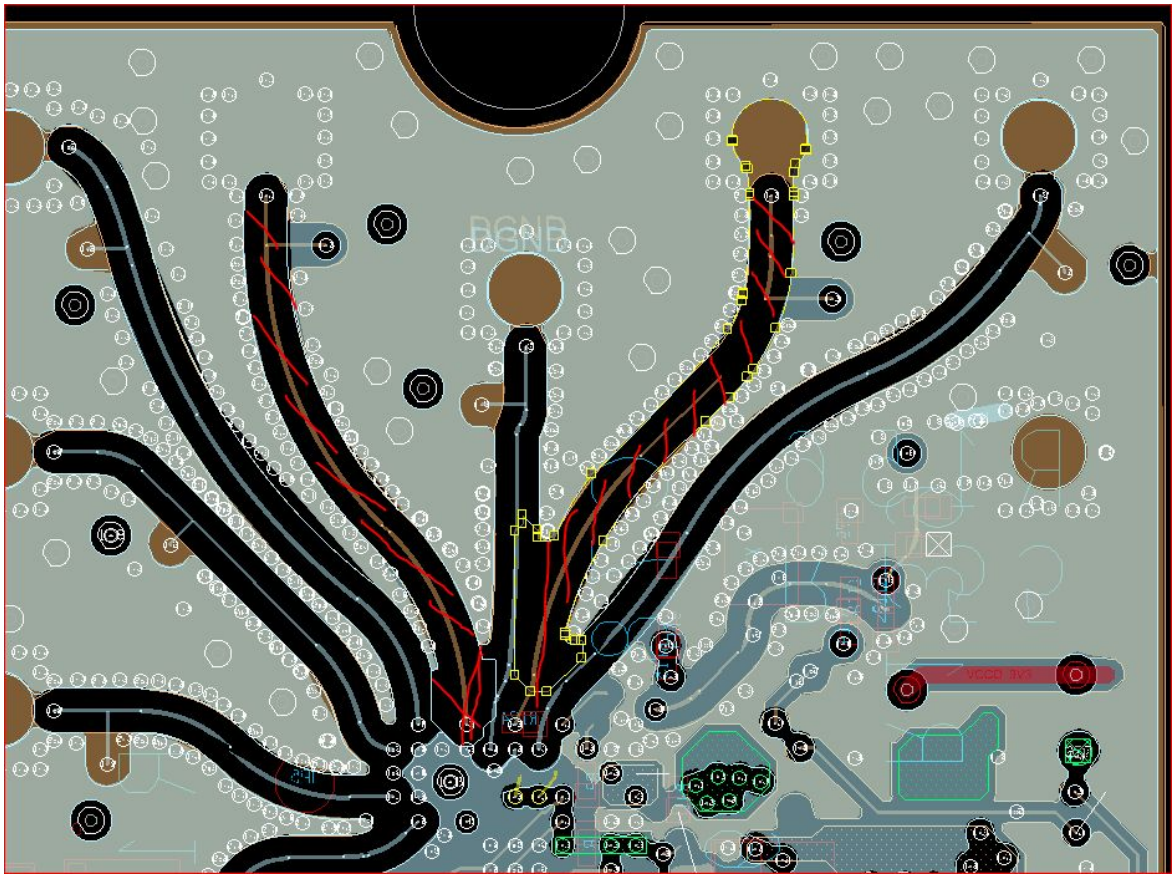
Nominal Thick.	Tolerance	LYR #	Single Ended Model Org. L/W	A/W L/W	Fin. L/W	Ref. Plane	Calc. Imp.	LYR #	Differential Model Org. L/W	Org. space	A/W L/W	A/W space	Fin. L/W	Fin. space	Ref. Plane	Calc. Imp.	K Factor Zs	Ks	ZD	KD
43.18		1	77		77	2	50	1	72	250			72	250	2	100				
								1	100	180			100	180	2	85				
53.34																				
16.51																				
60.96																				
26.67		3	70		70	2 & 4	50	3	70	250			70	250	2 & 4	100				
								3	95	180			95	180	2 & 4	85				
113.03																				
16.51																				
101.60																				
16.51																				
113.03																				
26.67		6	70		70	5 & 7	50	6	70	250			70	250	5 & 7	100				
60.96								6	95	180			95	180	5 & 7	85				
16.51																				
53.34																				
								8	100	180			100	180	2	85				
43.18		8	77		77	7	50	8	72	250			72	250	7	100				

Thickness After plating	762.00	not including solder mask	Units	Um	
Target Thickness	0.8 ± 0.100	over Plating	Impedance Tolerance	(SE) +/- 10%	(DIFF) +/- 15%

XIF Trace on Layer 3 – fill Layer 2

Route on L3 with L2 full reference above (ref layers L2 and L4)

Ned stackup allow this new routing



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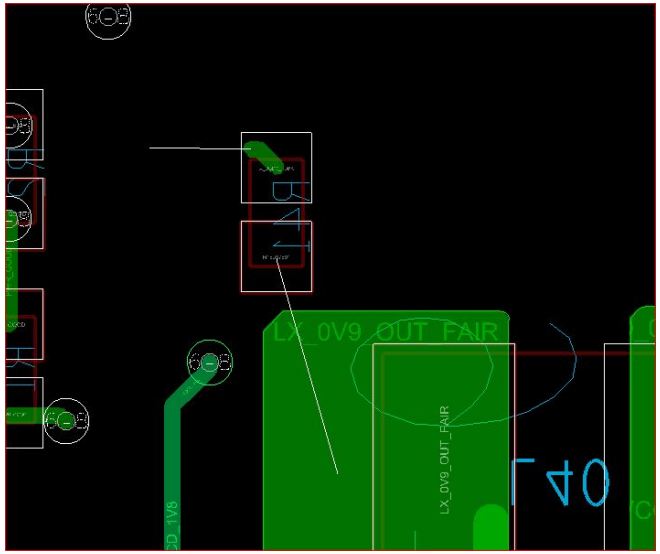
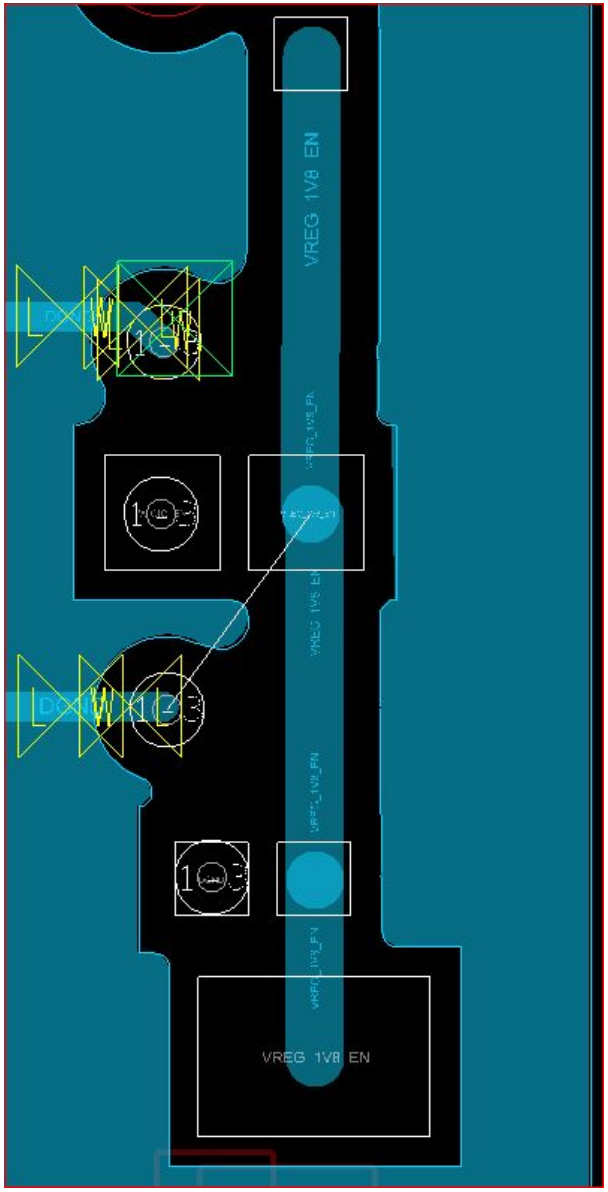
Netlist change

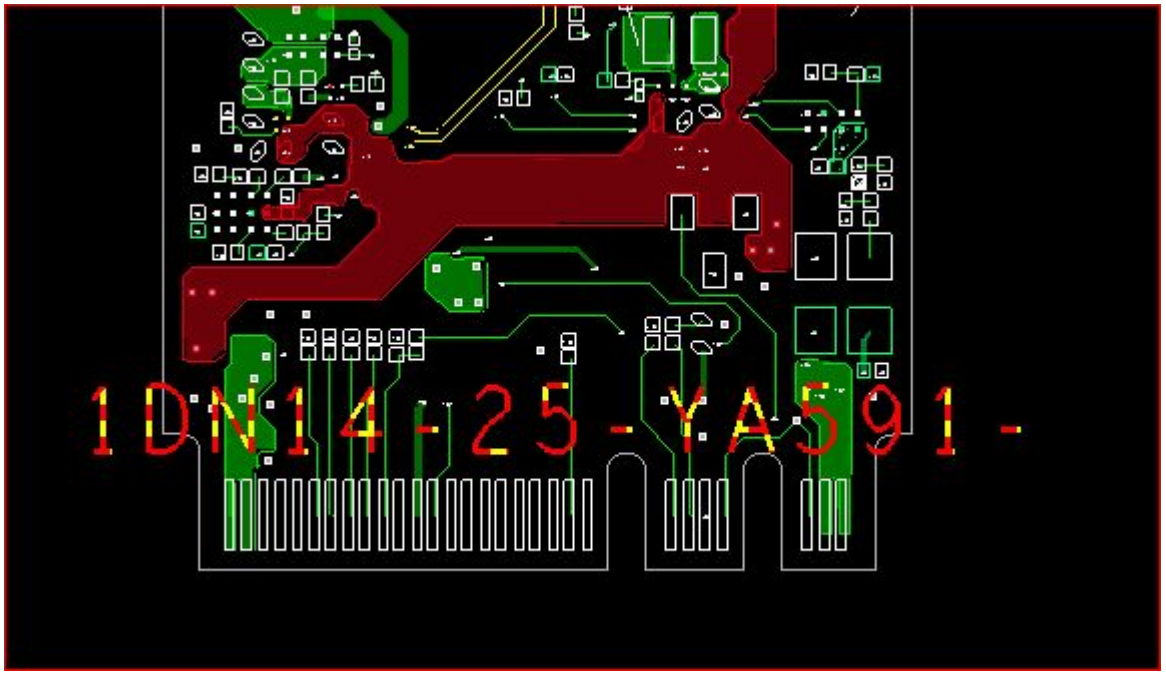
Fix open nets – I removed several components





Silk screen

Make the bottom side label smaller to fit the



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